Chapter 1

2 MARKS QUESTIONS

1.What do you mean by radix of a number . [2013,2016, 2018 (W)]

The radix of a number system is defined as the number of different digits which can occur in each position in the number system for example :Decimal number system has a base or radix of 10 .

2.Convert (11101101) from gray to binary code .[2013]

Gray11101101

Binary10110110

3.Substrate 0111 from 1111 by using 2's complement method. [2014]

Now 1111-0111=?

Now we have to write the 2's complement of 0111 is 1001

Now add 1111+1001=1000

Ans is 1000

4. Convert the following number into gray codes

a)1101011 b)100010110 [2015]

a)binary 1101011

gray 1011110

The gray code is 1011110

b)binary 100010110

gray 110011101

The gray code is 110011101

5.What is self correcting code ?[2015,2016]

Self correcting code or humming code detects an error and indicates which bit is in error .This incorrect bit then can be changed to its correct form .This code is used for correcting a single error on a message of length .

6 .Find the 2's complement of a number 11001011.[2015]

Number is 110010110,then convert it into 1's complement i.e 00110100

After that add 1 with that 1's complement 00110100+1=00110101

7.what is thedifference between weighted and non-weighted codes?give at least the example of each code.[2018(W)]

Particulars	Weighted Codes	Non-weighted Codes
Weight	In this code,each bit position is assigned a specific weight.	In this case, no specific weight are assigned to the bit position
Value	Each bit position represents a fixed value.	Each position within the binary number is not assigned any fixed value.
Exaplme	BCD, 8421, 5211, 6421	Excess-3 code and Gray code
Application	1. Data manipulation during arithmatic operation 2. for input output operation in digital circuit. 3. To represent the decimal digits in calculators, volt meter etc.	1. To perform certain arithmatic operation. 2. Shift position encodes. 3. Used for error detecting purpose.

8.perform BCD addition of (204.6+185.56).[2018 (W)]

Binary form:204.6=0010 0000 0100.0110 0000

+ 185.56=0001 1000 0101.0101 0110

0011 1000 1001.1011 0110

9. Convert (11100101)gray code to binary.[2018(W)]

gray code: 11100101

binary code: 10111001

10.perform 2's complement subtraction of(12-15). [2018(W)]

12=1100

15=1111 2's complement of(1111)will be0001

12-15= 1100

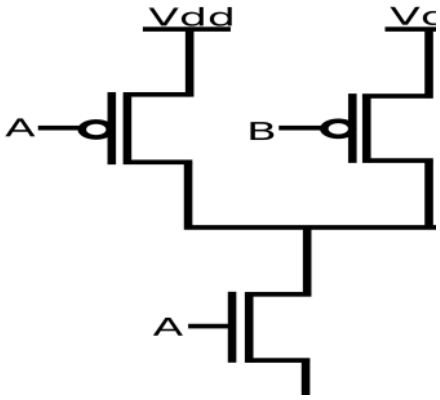
0001

1101

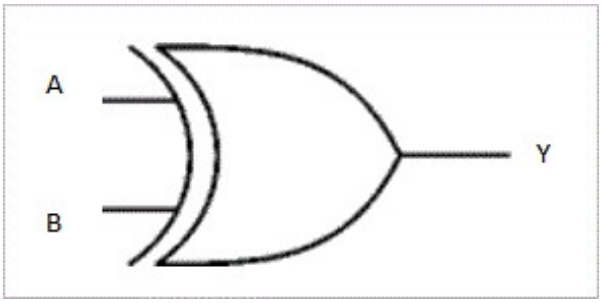
Chapter 2

2 MARKS QUESTIONS

1.Draw CMOS logic circuit of nand gate .[2014]



2. Write down the truth table for a two input ex-or gate.[2018(W)]



INPUTS		OUTPUTS
A	B	$Y = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

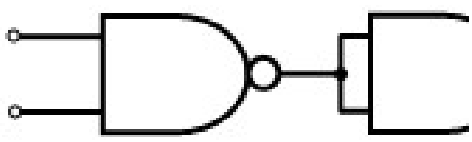
7 MARKS QUESTIONS

1 .Which gate are referred as universal gate and how gates can be realised using NAND gate. [2013,2014,2015,2016,2018(W)]

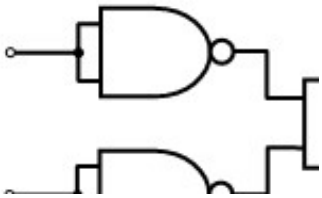
- NAND gate and NOR gate are known as universal logic gates .All logic gates are implemented using NAND and NOR gate only.

Implementation of all logic gates by using NAND gate :-

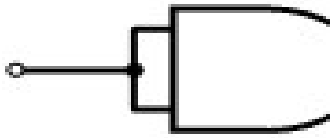
AND gate using NAND gate :-



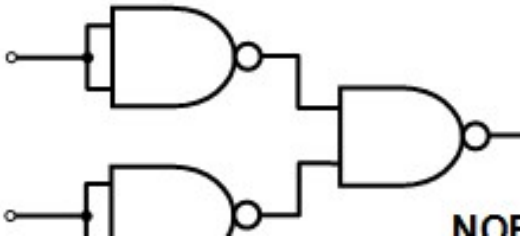
OR gate using NAND gate :-



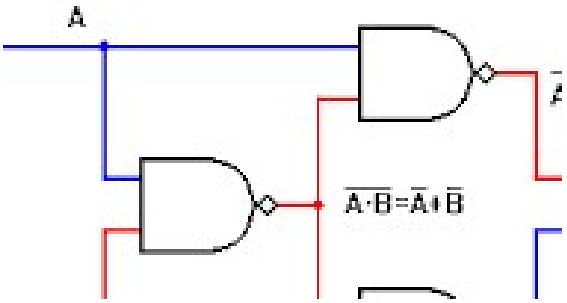
Not gate using NAND gate :-



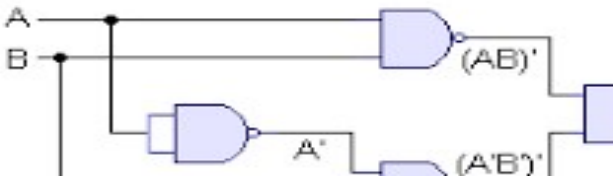
NOR gate using NAND gate :-



Ex –OR gate using NAND gate :-



EX-NOR gate using NAND gate :-



Chapter 3

2 MARKS QUESTIONS

1.Define Dont't care condition .[2014]

A variable that signified in a function table as don't care or X can take on either value HIGH or LOW without having any effect on the output .Thus donot care variable can be ignored .

2.State De-morgan's theorem. [2015,2016,2018(W)]

This law states that the complement of any expression can be obtained by replacing each variable and element with its complement and changing OR operators to AND operators and AND operators to OR operators .These can be expressrd as follows .

i) $\overline{A + B} =$

5 MARKS QUESTIONS

1.State and prove de-morgan's theorem[2014]

To prove

$$\overline{A+B} = \bar{A}.\bar{B}$$

Since each variable can have a value either 0 or 1, the following four cases arise:

(i) *When* $A = 0, \quad B = 0,$

$\overline{A+B} = \overline{0+0} = \bar{0} = 1$

and $\bar{A}.\bar{B} = \bar{0}.\bar{0} = 1.1 = 1$

Hence $\overline{A+B} = \bar{A}.\bar{B}$

(ii) *When* $A = 0, \quad B = 1,$

$\overline{A+B} = \overline{0+1} = \bar{1} = 0$

and $\bar{A}.\bar{B} = \bar{0}.\bar{1} = 1.0 = 0$

Hence $\overline{A+B} = \bar{A}.\bar{B}$

(iii) *When* $A = 1, \quad B = 0,$

$\overline{A+B} = \overline{1+0} = \bar{1} = 0$

and $\bar{A}.\bar{B} = \bar{1}.\bar{0} = 0.1 = 0$

Hence $\overline{A+B} = \bar{A}.\bar{B}$

(iv) *When* $A = 1, \quad B = 1,$

$\overline{A+B} = \overline{1+1} = \bar{1} = 0$

and $\bar{A}.\bar{B} = \bar{1}.\bar{1} = 0.0 = 0$

Hence $\overline{A+B} = \bar{A}.\bar{B}$

Since, in every case the left hand side equals the right hand side, the theorem is proved.

To prove

$$\overline{A \cdot B} = \bar{A} + \bar{B}$$

Since each variable can have a value either 0 or 1, the following four cases arise:

(i) *When* $A = 0, \quad B = 0,$

$\overline{A \cdot B} = \overline{0 \cdot 0} = \bar{0} = 1$

and $\bar{A} + \bar{B} = \bar{0} + \bar{0} = 1 + 1 = 1$

Hence $\overline{A \cdot B} = \bar{A} + \bar{B}$

(ii) *When* $A = 0, \quad B = 1,$

$\overline{A \cdot B} = \overline{0 \cdot 1} = \bar{0} = 1$

and $\bar{A} + \bar{B} = \bar{0} + \bar{1} = 1 + 0 = 1$

Hence $\overline{A \cdot B} = \bar{A} + \bar{B}$

(iii) *When* $A = 1, \quad B = 0,$

$\overline{A \cdot B} = \overline{1 \cdot 0} = \bar{0} = 1$

and $\bar{A} + \bar{B} = \bar{1} + \bar{0} = 0 + 1 = 1$

Hence $\overline{A \cdot B} = \bar{A} + \bar{B}$

(iv) *When* $A = 1, \quad B = 1,$

$\overline{A \cdot B} = \overline{1 \cdot 1} = \bar{1} = 0$

and $\bar{A} + \bar{B} = \bar{1} + \bar{1} = 0 + 0 = 0$

Hence $\overline{A \cdot B} = \bar{A} + \bar{B}$

As all possible combinations of A and B are exhausted, the theorem is proved.

2. Simplify the Boolean expression by Boolean algebra and draw the logic circuit by using NAND gate.[2015]

$$X=AB+\bar{A}C+A\bar{B}C(AB+C)'$$

$$=AB+\bar{A}C+A\bar{B}C.AB+A\bar{B}C.C$$

$$=AB+\bar{A}C+A\bar{B}C \qquad [\because A.\bar{A}=0$$

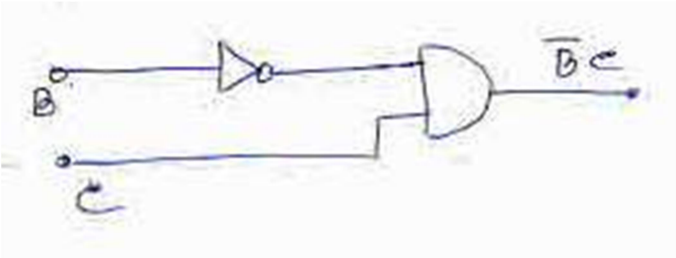
$$=AB+C(\bar{A}+A\bar{B}) \qquad [\because A+\bar{A}B=A$$

$$=AB+C(\bar{A}+\bar{B})$$

$\overline{A\,B}=\bar{A}+\bar{B}$ $\qquad$ $\overline{\bar{A}+\overline{B.C}}$

3.simplify the boolean expression.[2018(W)]

Y=[AB'(C+BD)+A'B']C and draw the logic circuit for the simplified expression.



y=[AB'(C+BD)+A'B']C

=[AB'C+AB'.BD+A'B']C (B.B'=0)

=[AB'C+A'B']C

=AB'C+A'B'C

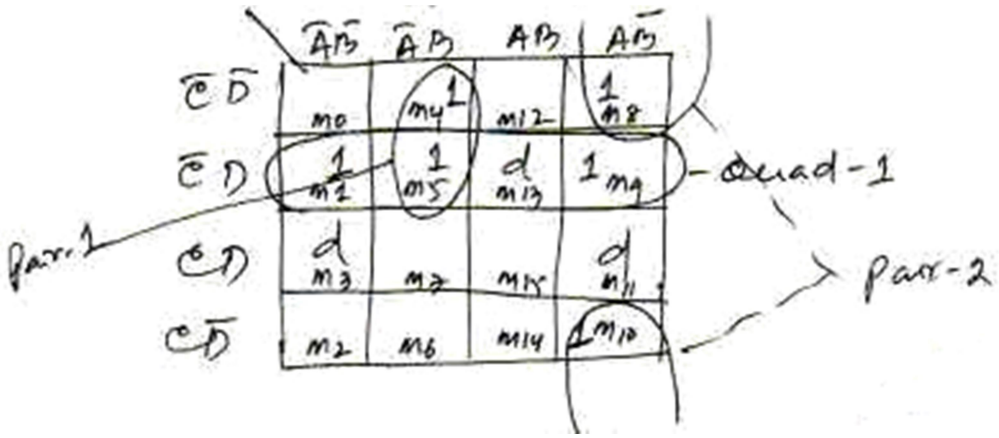
=B'C(A+A')

=B'C (A+A'=1)

Y=B'C

4. Simplify the given expression using Karnaugh's map and draw the logic circuit using universal gates:-F(A, B, C, D) = $\sum_m$ (1, 4, 5, 8, 9, 10) + d(3, 11, 13) [2018(W)]

Ans:-

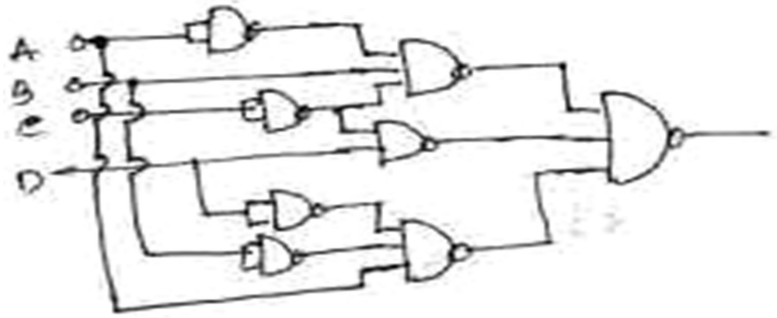


Quad 1 is reduced to $\overline{C}D$

Pair 1 is reduced to $\overline{A}B\overline{C}$

Pair 2 is reduced $A\overline{B}\overline{D}$

Hence $F(A, B, C, D) = \overline{C}D + \overline{A}B\overline{C} + A\overline{B}\,\overline{D}$



Chapter 4

2MARKS QUESTIONS

1.Define combinational logic circuit. [2014]

- The combinational logic circuit or time independent logic circuits in digital circuit theory can be defined as a type of digital logic circuit implemented using Boolean circuits ,where the output of logic circuit is a pure function of the present inputs only .
- The combinational logic circuit operation is instantaneous and these circuits do not have the memory or feedback loops .

2.What is a multiplexer and decoder ?[2015]

- The term ‘multiplex’ means “many into one “.Multiplexing is the process of transmitting a large number of information over a single line .
- A decoder is a combinational circuit that converts binary information from n inputs lines to a maximum of 2^n unique output lines .

5 MARKS QUESTIONS

1.Design a 4:2 encoder with neat circuit diagram. [2013, 2015]

An encoder is a digital circuit that performs the inverse operation of a decoder .

An encoder has 2^n input lines and n numbers of output lines .

4:2 encoder :

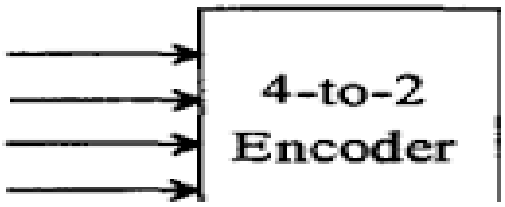
Input=2^n=4(I_0,I_1,I_2,I_3)

Output=n=2(D_0 ,D_1)

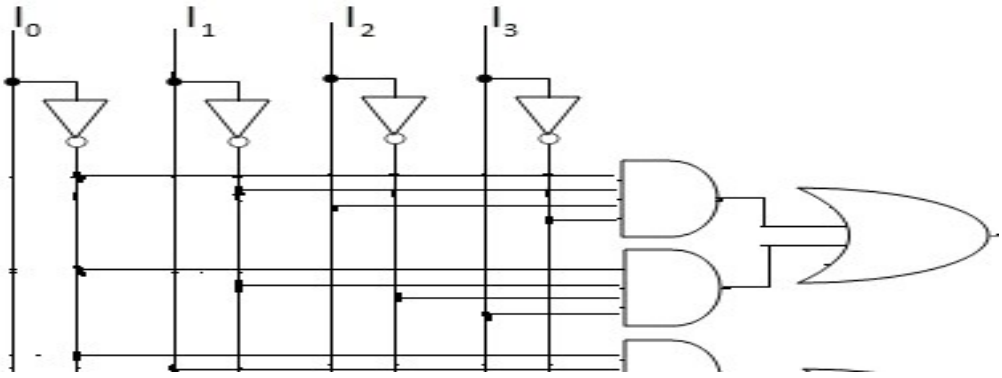
Truth table :-

input				
I_0	I_1	I_2	I_3	
1	0	0	0	
0	1	0	0	

Block diagram :-



Logic diagram :-



2.Write sop and pos form of Boolean expression of F(A,B,C)=Σ(0 ,1 ,3 ,5,7) .[2014]

Truth table :-

A	B	C	ou
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	

Sop expression is :

$$SOP(X)=\bar{A}\,\bar{B}\,C+A\,\bar{B}\,C+A\,B\,\bar{C}+A\,\bar{B}\,\bar{C}+A\,B\,C$$

$$=\bar{A}\,\bar{B}(C+\bar{C})+B\,C(A+\bar{A})+A\,\bar{B}\,\bar{C}$$

$$=\bar{A}\,\bar{B}+B\,C+A\,\bar{B}\,\bar{C}$$

$$=\bar{A}\,\bar{B}+C(B+A\,\bar{B})$$

Pos expression is :

$$POS(Y)=PI(2,4,6)$$

$$=(A+\bar{B}+C)(\bar{A}+B+C)(\bar{A}+\bar{B}+C)$$

$$=(A+\bar{B}+C)\{\bar{A}+C+(B.\bar{B})\}$$

$$=(A+\bar{B}+C)(\bar{A}+C+0)$$

$$=C+(A+\bar{B}).\bar{A}$$

$$=\bar{A}\,\bar{B}+C$$

<u>3.Explain briefly 1:4 de-mux with neat diagram .</u>[2014 ,2015,2018(W)]

Here number of input is 1

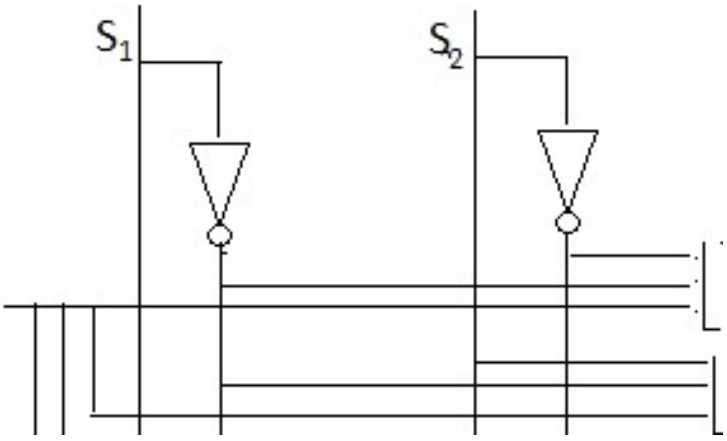
Number of output is n=2

Number of output $=2^n=4$

Truth table :-

inputs	Selection lines	
	S_1	S_0
I	0	0
	0	1

$Y_0=\bar{S}_0\bar{S}_1 I$, $Y_1=\bar{S}_0 S_1 I$, $Y_2=S_0\bar{S}_1 I$, $Y_3=S_0 S_1 I$



4.<u>Explain with neat circuit diagram 4:1 multiplexer .</u>[2016,2018(W)]

4 :1 mux =2^2:1 mux

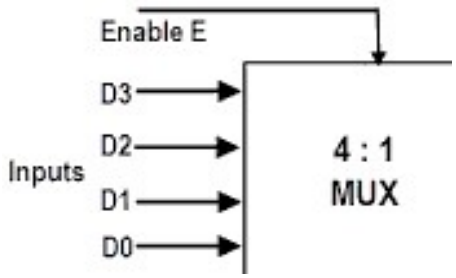
Here number of inputs =2^n =4(D_0 ,D_1,D_2,D_3)

Number of selection line ,n =2 (S_1 ,S_0)

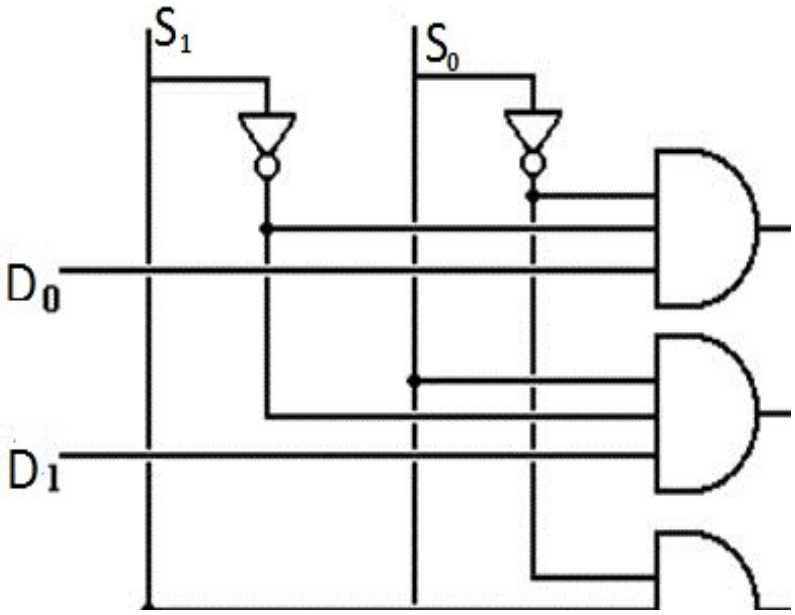
Truth Table :-

Data select inputs		(
S_1	S_0	
0	0	
0	1	

Block diagram :-



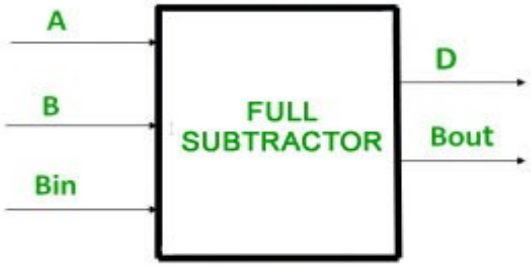
Circuit diagram :-



5.Describe the operation of full subtractor with the help of truth table and circuit diagram. [2018(W)]

Full subtractor is an electronic device or logic circuit which performs subtraction of two binary digits. It is a combinational logic circuit used in digital electronics.A full subtractor is formed by two half subtractors, which involves three inputs such as minuend, subtrahend and borrow, borrow bit among the inputs is obtained from subtraction of two binary digits and is subtracted from next higher order pair of bits, outputs as difference and borrow.

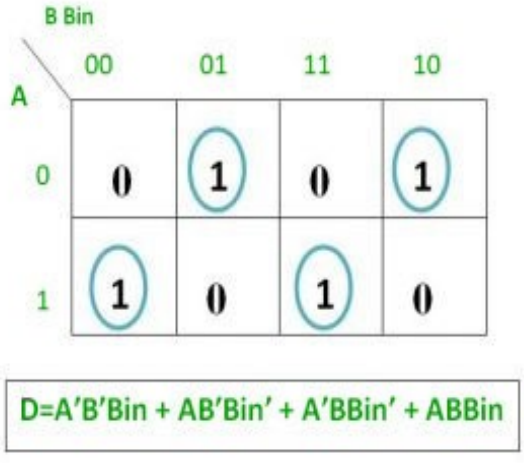
Full Subtractor Block Diagram:



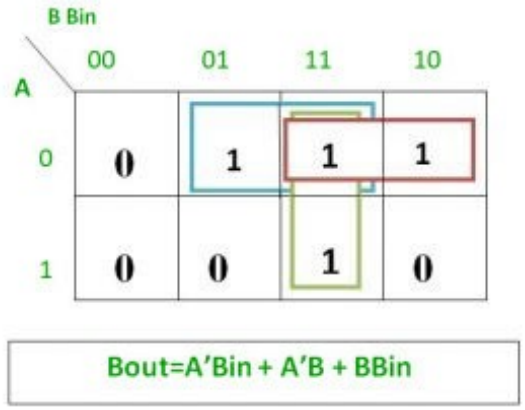
Truth table for full subtractor:

INPUT			OUTPUT	
A	B	Bin	D	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

K-map for difference:



K-map for borrow:



Logical expression for difference :

D = A'B'Bin + A'BBin' + AB'Bin' + ABBin

= Bin(A'B' + AB) + Bin'(AB' + A'B)

= Bin(A XNOR B) + Bin'(A XOR B)

= Bin (A XOR B)' + Bin'(A XOR B)

= Bin XOR (A XOR B)

= (A XOR B) XOR Bin

Logical expression for borrow :

Bout = A'B'Bin + A'BBin' + A'BBin + ABBin

= A'B'Bin +A'BBin' + A'BBin + A'BBin + A'BBin + ABBin

= A'Bin(B + B') + A'B(Bin + Bin') + BBin(A + A')

= A'Bin + A'B + BBin

OR

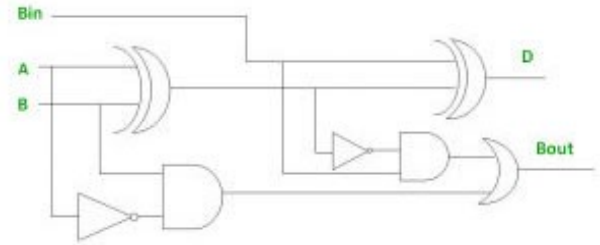
Bout = A'B'Bin + A'BBin' + A'BBin + ABBin

= Bin(AB + A'B') + A'B(Bin + Bin')

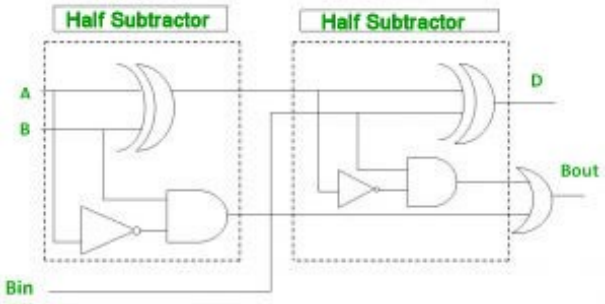
= Bin(A XNOR B) + A'B

= Bin (A XOR B)' + A'B

Circuit diagram for full subtractor:

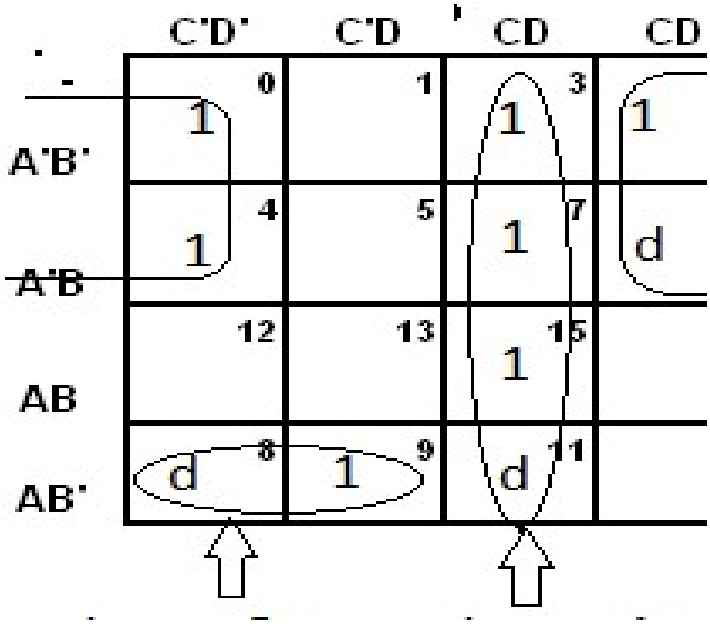


Full subractor using two half subtractor:

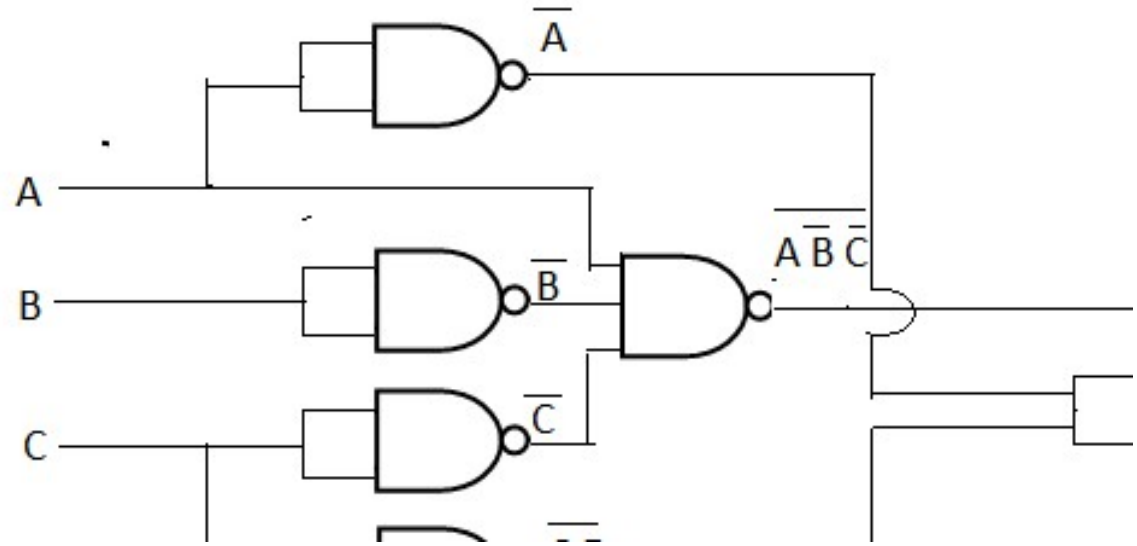


7 MARKS QUESTIONS :-

1.Simplify the given expression using K-map and draw the logic circuit using NAND gate only .F(A ,B ,C ,D)=Σ (0 ,2 ,3 ,4 ,7 ,9 ,15)+d(6,8,11) [2013]



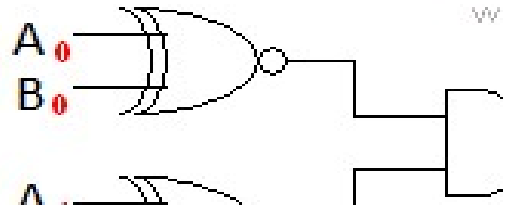
Logic diagram :-



2.Design a 2 bit magnitude comparator whose output are A>B ,A+B and A<B where A and B are 2 bit numbers .[2013 ,2015 ,2016,2018(w)]

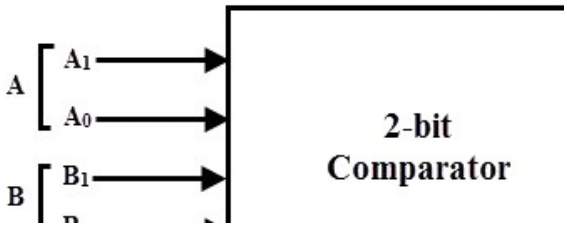
In the evaluation of digital information it is important to compare two binary strings (or binary word say A ,B)to determine is they are exactly equal .This is done by using digital comparators.

Let us consider a 2 bit digital comparator as shown in figure .



The inputs are A1 ,A0 and B1 ,B0 outputs are three states :A>B ,A+B and A<B .The logic gates are XNOR if both the bits are equal i.e 0-0 or 1-1 ,the XNOR outputs are 1 .

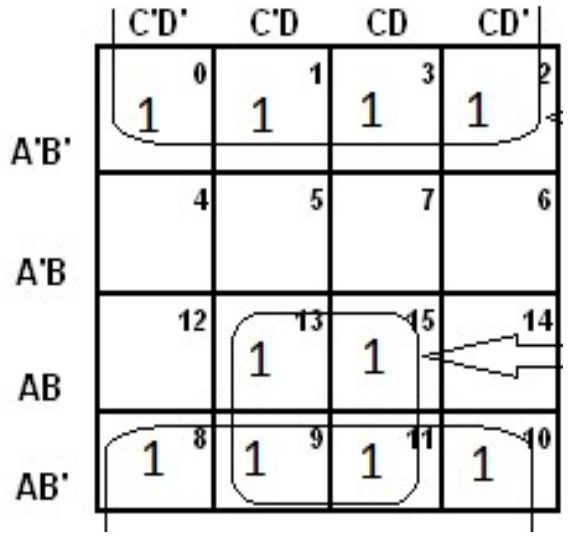
Block diagram :-

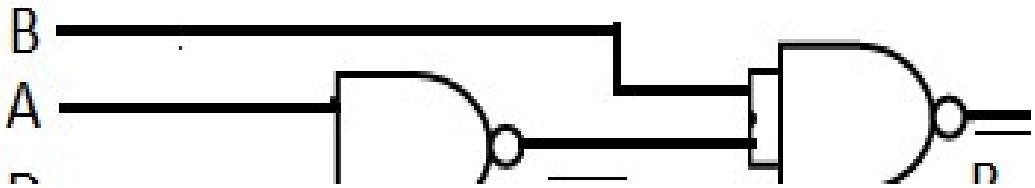


Truth Table :-

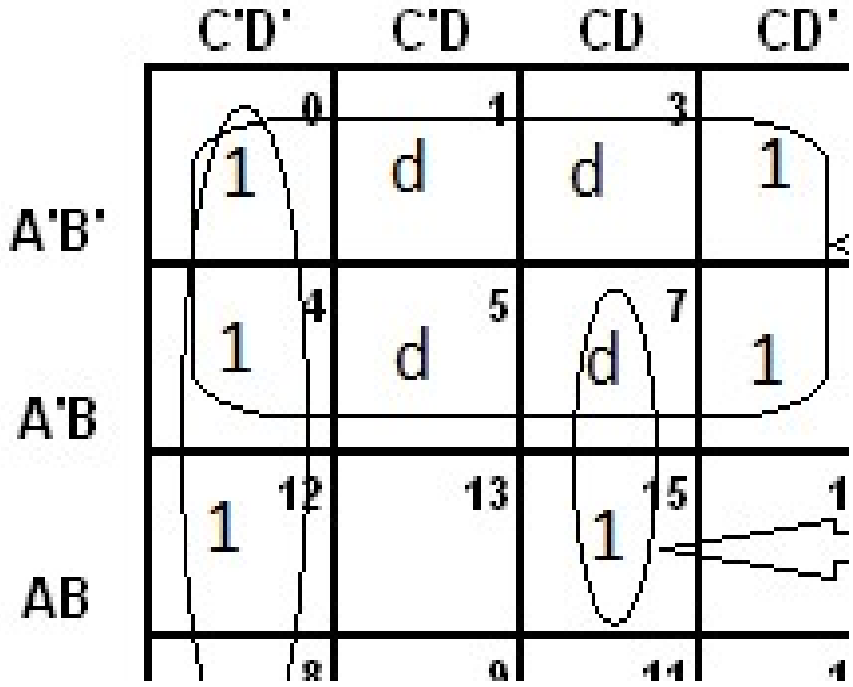
Inputs				
A		B		G(A>B)
A1	A0	B1	B0	
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1

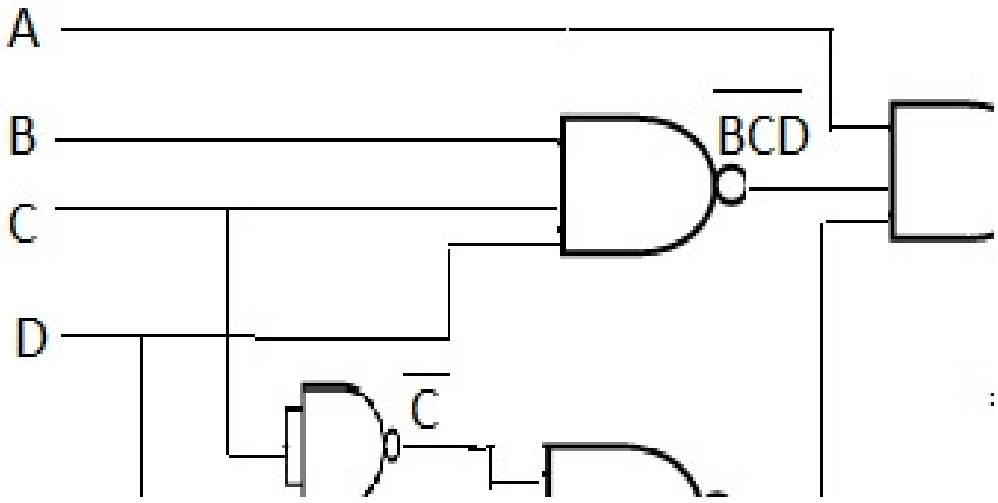
3.Simplify the Boolean expression using k-map F(A ,B ,C .D) =Σ(0,1,2,3,8,9,10,11,13,15) and draw its logic circuit using NAND gate. [2014] .





4.Simplify and minimize the 4 variable logic expression by using K-map and implement this circuit by using NAND gates. F(A,B,C,D)=Σ(0 ,2,4,6,8,12,15) +d (1,3,5,7) [2016]





5.Draw the logic circuit of a full adder .Give its logic expression and truthtable and implement the logic circuit with universal gates .[2014 ,2016]

It will perform the addition operation of three binary bits .

Truth table :-

INPUTS			
X	Y	Z	
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	

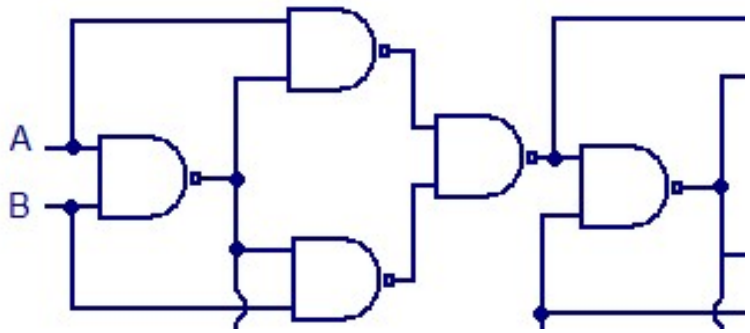
$$S = \overline{X}\,\overline{Y}\,Z + X\,\overline{Y}\,\overline{Z} + X\,\overline{Y}\,\overline{Z} +$$

$$\overline{X}\,(\overline{Y}\,Z + Y\,\overline{Z}) + X\,(\overline{Y}\,\overline{Z} +$$

$$\overline{X}\,(Y \oplus Z) + X\,(\overline{Y \oplus Z})$$

$$X \oplus [\,Y \oplus Z]$$

$$X \oplus Y \oplus Z$$



Chapter 5

2MARKS QUESTIONS

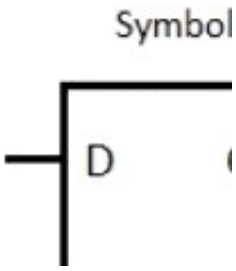
1.What is racing condition ?[2013 ,2014,2016,2018(W)]

- A race condition is an undesirable situation that occurs when a device or system attempts to perform two or more operations at the same time, but because of the nature of the device or system, the operations must be done in the proper sequence to be done correctly.
- A simple example of a race condition is a light switch. In some homes there are multiple light switches connected to a common ceiling light. When these types of circuits are used, the switch position becomes irrelevant

2.What is flipflop ?[2016]

- n electronics, a **flip-flop** or **latch** is a circuit that has two stable states and can be used to store state information. A flip-flop is a bistable multivibrator. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs.
- It is the basic storage element in sequential logic. Flip-flops and latches are fundamental building blocks of digital electronics systems used in computers, communications, and many other types of systems

3.Draw the truth table for D-flipflop [2016]



Inputs		
CLK	D	Q_{n+1}
0	d	Q_n
1	0	0

5 MARKS QUESTIONS :

1.Convert a)SR flip flop to D flip flop

b)JK flip flop to T flipflop[2013]

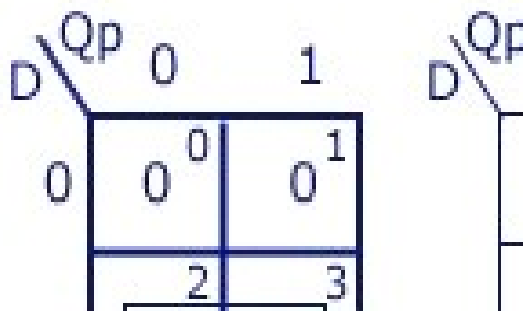
SR Flip Flop to D Flip Flop

As shown in the figure, S and R are the actual inputs of the flip flop and D is the external input of the flip flop. The four combinations, the logic diagram, conversion table, and the K-map for S and R in terms of D and Qp are shown below

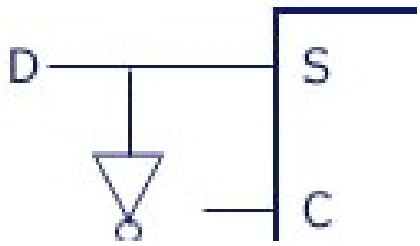
Conversion Tat

D Input	Outputs Qp	Qp+1
0	0	0
0	1	0

K-maps



Logic Diagram

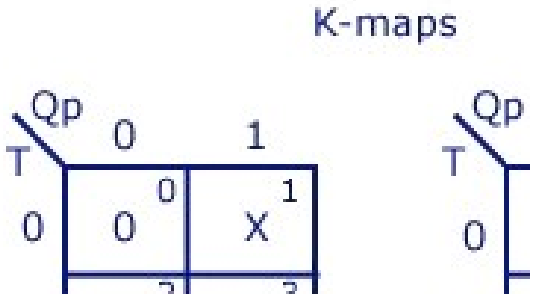


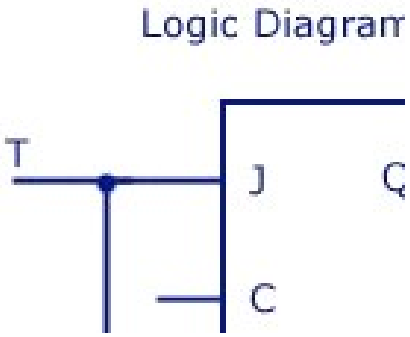
JK Flip Flop to T Flip Flop

J and K are the actual inputs of the flip flop and T is taken as the external input for conversion. Four combinations are produced with T and Qp. J and K are expressed in terms of T and Qp. The conversion table, K-maps, and the logic diagram are given below.

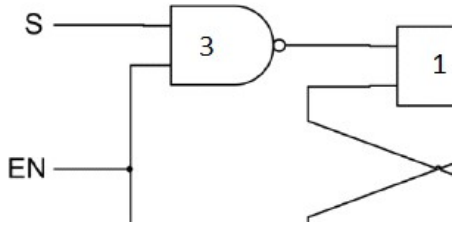
Conversion Table

T Input	Outputs Qp	Qp+1	J-K
0	0	0	0
0	1	1	X





2.Explain the working of clocked sr flipflop using NAND gate.[2013 ,2014 ,2015]



Truth Table :-

Inputs			Outputs		Mod
clk	S	R	Q	Q	
1	0	0	no change		
1	0	1	0	1	

In the functional table the explanation is given below :

Let R=S=1 ,Clk=1 ,the output of gates 3 ,4 are both 0 ,making one of the inputs of gate 1 and 2 NAND gates 0.As a result the output Q and Q both will attain high 1 which is in consistent .

For R=0 ,S=1 ,clk =1 ,the output is high i.e Q=1 and Q=0 which is a condition that the flipflop is set

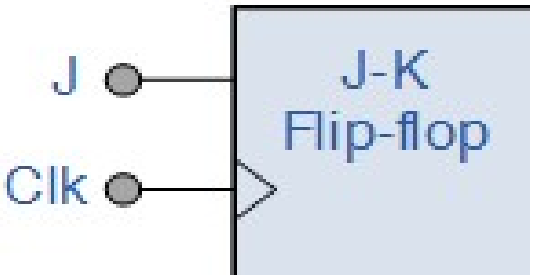
For R=1 ,S=0 ,Clk=1 ,the output is low i.e Q=0 and Q=1 ,which shows reset condition .For R=0 ,S=0 ,Clk=1 ,the output remains same i.e do not change .

3.Differentiate between latches and flipflops and explain working of JK flipflop with neat diagram .[2015]

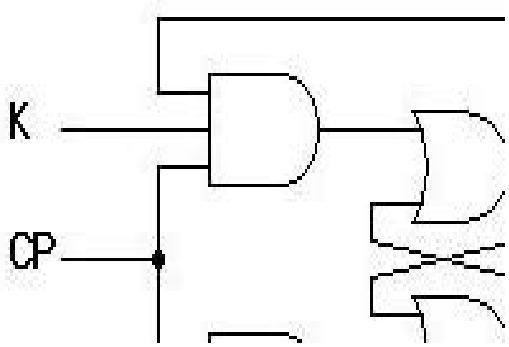
Latches	
Latches are building blocks of sequential circuits and these can be built from logic gates	Flip flops ar sequential cir from the latcl
Latch continuously checks its inputs and changes its output correspondingly.	Flip flop con and changes only at time signal
The latch is sensitive to the duration of the pulse and can send or receive the data when the switch is on	Flipflop is se They can trar instant and d: next signal ch register.

4.Show the diagram of a clocked JK flipflop .Explain its working with a functional table .[2016,2018(w)]

The JK flip-flop is probably the most widely used and is considered the universal flip-flop because it can be used in many ways.



Circuit diagram :



The JK flipflop has two inputs J and K .It is the improved version of RS flipflop so that when both inputs 1 then also the output Q and Q are complement to each other .

Truth table :-

Truth Table

J	K	CLK	Q
0	0	↑	Q_0(no
1	0	↑	1

Working Principle :-

- When J and K both are low ,both AND gates are disolbed and there is no effect of clock pulse and the output remains what it was before the arrived of the pulse
- When J is low and K is high the upper gate is disabled and the flipflop cannot be set and the output Q will be 0 i.e it will reset the flipfliop .
- When J is high and K is low the lower gate will be disabled and the flipflop cannot be reset
- When J and K both are high we can set or reset the flipflop depending upon its position at present when J and K both are high what ever may be the output ,it will change to its complement i.e if it is 0 then it change to 1 and if it is 1 then it change to 0 and the condition of flipflop is known as toggle .

5.Distinguish between combinational logic and sequential logic circuit [2016,2018(W)]

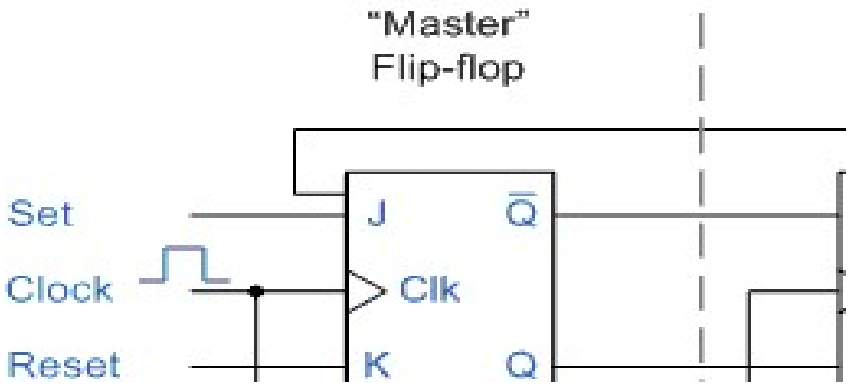
Difference between Combi
sequential circuit

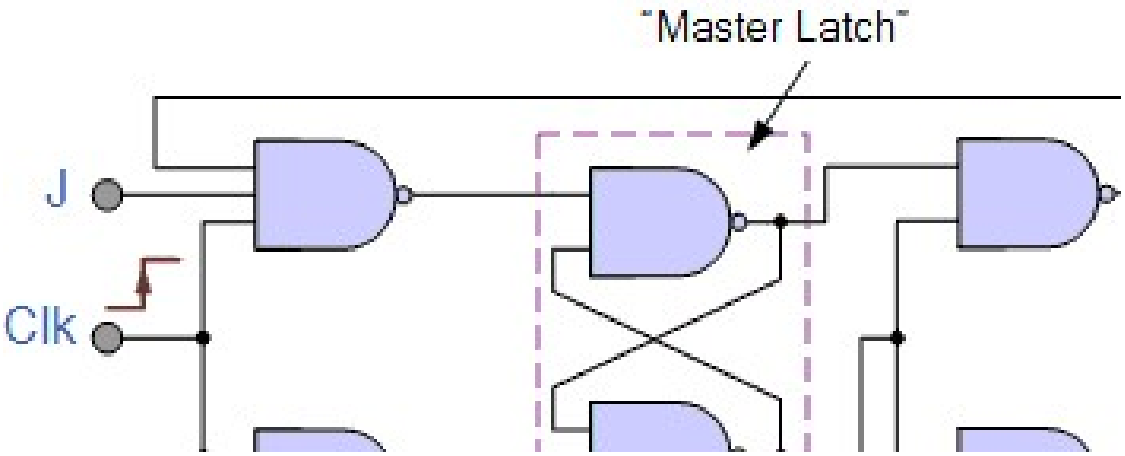
Combinational	Sequentia
Output of any instance of time depends only upon the input variables	Output is g upon the p and also o history of t
Memory unit is not required. i.e. it doesn't allocate any memory to the elements.	Memory u allocates a elements.
Faster	Slower

7 MARKS QUESTIONS

1.Draw the circuit diagram of master slave JK flipflop .Explain it with a functional table [2013 ,2016]

Master-slave flip flop is designed using two separate flip flops. Out of these, one acts as the master and the other as a slave. The figure of a master-slave J-K flip flop is shown below.

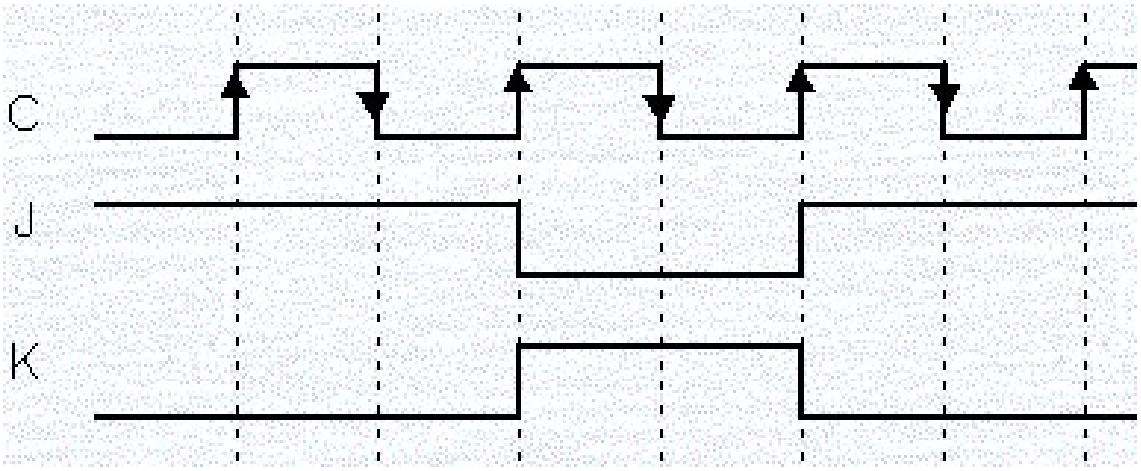




From the above figure you can see that both the J-K flip flops are presented in a series connection. The output of the master J-K flip flop is fed to the input of the slave J-K flip flop. The output of the slave J-K flip flop is given as a feedback to the input of the master J-K flip flop. The clock pulse [Clk] is given to the master J-K flip flop and it is sent through a NOT Gate and thus inverted before passing it to the slave J-K flip flop.

Working

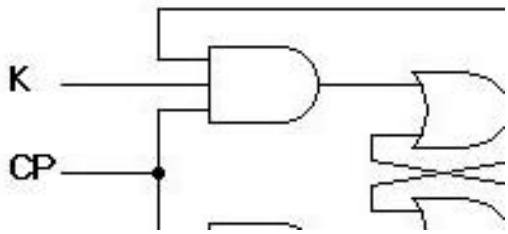
- When Clk=1, the master J-K flip flop gets disabled. The Clk input of the master input will be the opposite of the slave input. So the master flip flop output will be recognized by the slave flip flop only when the Clk value becomes 0. Thus, when the clock pulse males a transition from 1 to 0, the locked outputs of the master flip flop are fed through to the inputs of the slave flip-flop making this flip flop edge or pulse-triggered.
- thus, the circuit accepts the value in the input when the clock is HIGH, and passes the data to the output on the falling-edge of the clock signal. This makes the Master-Slave J-K flip flop a Synchronous device as it only passes data with the timing of the clock signal.



2 Explain the working of JK flipflop and how it convert to RS ,T and D flip flop .[2014]

The JK flipflop has two inputs J and K .It is the improved version of RS flipflop so that when both inputs 1 then also the output Q and Q are complement to each other .

Circuit diagram :



Truth table :-

Truth Table

J	K	CLK	Q
0	0	↑	Q_0(no
1	0	↑	1

Working principle :-

The JK flipflop has two inputs J and K .It is the improved version of RS flipflop so that when both inputs 1 then also the output Q and Q are complement to each other .

Working Principle :-

When J and K both are low ,both AND gates are disolbed and there is no effect of clock pulse and the output remains what it was before the arrived of the pulse

When J is low and K is high the upper gate is disabled and the flipflop cannot be set and the output Q will be 0 i.e it will reset the flipfliop .

When J is high and K is low the lower gate will be disabled and the flipflop cannot be reset

When J and K both are high we can set or reset the flipflop depending upon its position at present when J and K both are high what ever may be the output ,it will change to its complement i.e if it is 0 then it change to 1 and if it is 1 then it change to 0 and the condition of flipflop is known as toggle .

JK Flip Flop to SR Flip Flop

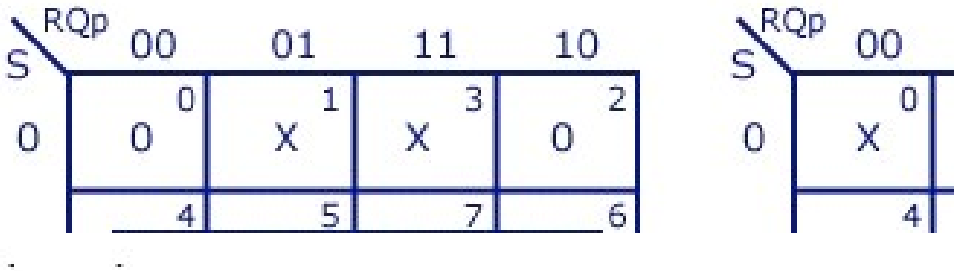
This will be the reverse process of the above explained conversion. S and R will be the external inputs to J and K. As shown in the logic diagram below, J and K will be the outputs of the combinational circuit. Thus, the values of J and K have to be obtained in terms of S, R and Qp. The logic diagram is shown below.

A conversion table is to be written using S, R, Qp, Qp+1, J and K. For two inputs, S and R, eight combinations are made. For each combination, the corresponding Qp+1 outputs are found ut. The outputs for the combinations of S=1 and R=1 are not permitted for an SR flip flop. Thus the outputs are considered invalid and the J and K values are taken as “don’t cares”.

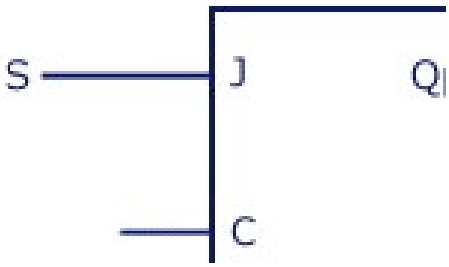
Conversion Table

S-R Inputs		Outputs	
S	R	Qp	Qp+1
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1

K-maps



Logic Diagrar



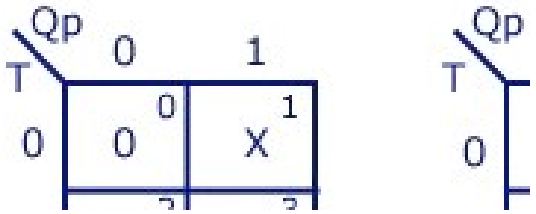
JK Flip Flop to T Flip Flop

J and K are the actual inputs of the flip flop and T is taken as the external input for conversion. Four combinations are produced with T and Qp. J and K are expressed in terms of T and Qp. The conversion table, K-maps, and the logic diagram are given below.

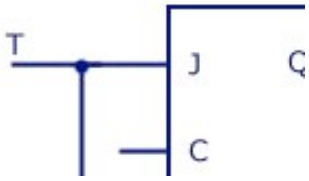
Conversion Table

T Input	Outputs Qp	Qp+1	J-K
0	0	0	0
0	1	1	X

K-maps



Logic Diagram



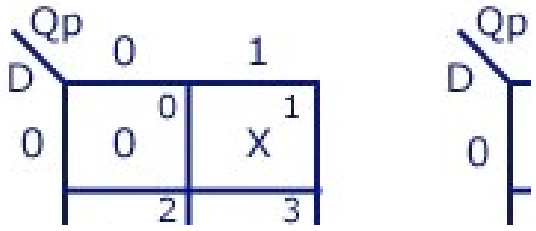
. **JK Flip Flop to D Flip Flop**

D is the external input and J and K are the actual inputs of the flip flop. D and Qp make four combinations. J and K are expressed in terms of D and Qp. The four combination conversion table, the K-maps for J and K in terms of D and Qp, and the logic diagram showing the conversion from JK to D are given below.

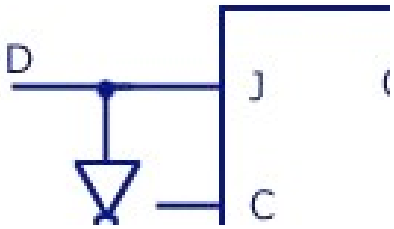
Conversion Table

D Input	Outputs Qp	Outputs Qp+1	J
0	0	0	
0	1	0	

K-maps



Logic Diagrar



3.Convert a) JK flipflop to D flip flop

b) SR flipflop to T flip flop

c) JK flipflop to SR flip flop

d) T flipflop to D flip flop [2015]

JK flipflop to D flip flop :

Previously done

SR-to-T Flip-Flop:

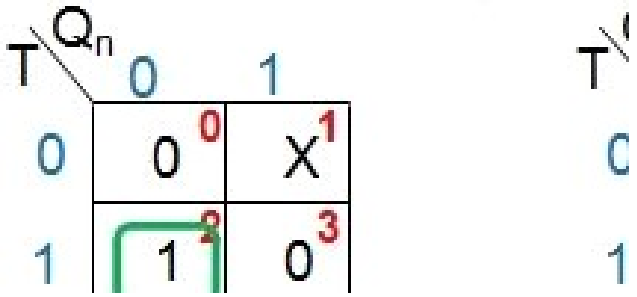
In order to convert the given SR flip-flop into T-type, we have to first write the SR-to-T conversion table, which is shown in Figure

Truth Table of T Flip-flop

Input	Outputs	
	Present State	Next State
T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1

T Input	Outputs		SR Inputs	
	Present State	Next State		
T	Q_n	Q_{n+1}	S	R
0	0	0	0	X
0	1	1	X	0
1	0	1	1	0

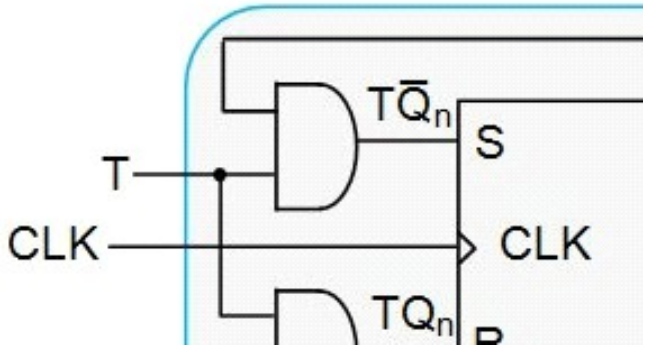
Now, we need to express the inputs S and R in terms of T and the present-state literal, Q_n. This can be accomplished by simplifying their logical expressions using the K-map technique



rom Figure 8, it can be noted that the SR flip-flop can be made to function as a T flip-flop with two actions:

- Connect the S input to the output of a two-input AND gate which is driven by the user-provided input, T, and the negation of the flip-flop's present-state, $\overline{Q}_n$
- Connect the R input to the output of a two-input AND gate which is driven by the user-defined input, T, and the present-state of the flip-flop, Q_n

Thus the resultant digital system would be as shown in Figure 9:



Now we shall check our conversion technique by writing the SR-to-T verification table, which is shown in Figure 10:

SR to T Verification Table

Input	Intermediate Inputs				Outputs	
T	Q	$\bar{Q}$	S = T$\bar{Q}$	R = TQ	Q	$\bar{Q}$
0	0	1	0	0	0	1
0	1	0	0	0	1	0
1	0	1	1	0	1	0

Tr

Input
T
0
0
1

Jk flip flop to SR flipflop:

Previously done

T to a D Flip-Flop:

Truth Table of D Flip-flop

Input	Outputs	
	Present State	Next State
D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1

D Input	Outputs		T Inpu
	Present State	Next State	
D	Q_n	Q_{n+1}	T
0	0	0	0
0	1	0	1
1	0	1	1

Once this is done, we need to express the input, T, in terms of the user-defined input, D, and the flip-flop's present-state, Q_n. We will again use the K-map simplification technique.

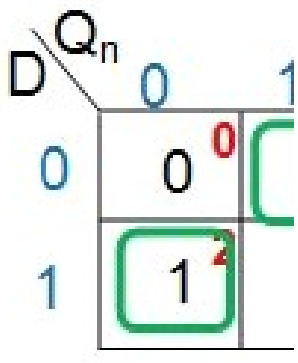
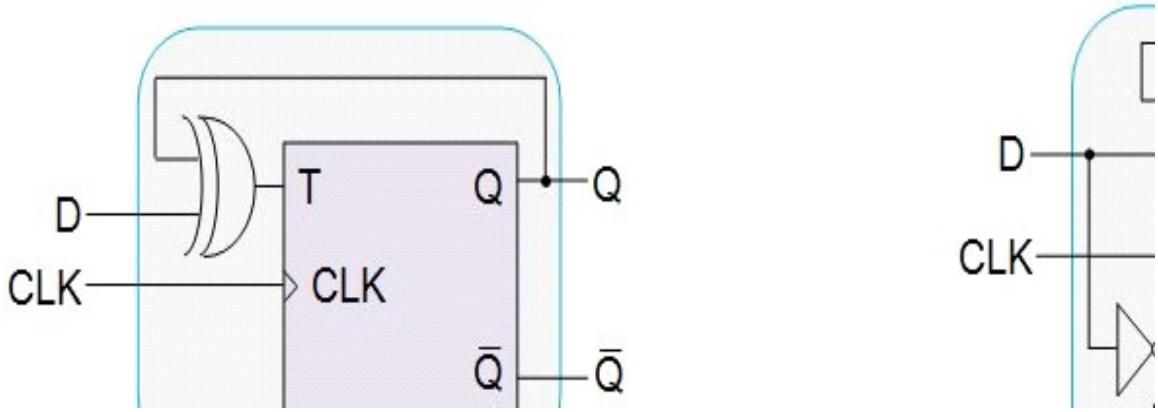


Figure 10 shows that, in order to make the given T flip-flop functionally equivalent to a D flip-flop, we need to drive its input pin, T, with the output of an XOR gate whose inputs are D and Q_n. This will lead to the new digital system shown in Figure 11(a). Figure 11(b) shows a system which is functionally equivalent to that of Figure 11(a) but is designed using only NOT, AND, and OR gates.



Finally, in order to ensure that the designed system behaves as expected, we will write a T-to-D verification table, shown in Figure 12.

T to D Verification Table

Input	Intermediate Inputs			Outputs	
D	Q	$\bar{Q}$	$T = D \oplus Q$	Q	$\bar{Q}$
0	0	1	0	0	1
0	1	0	1	0	1
1	0	1	1	1	0

Tr

Input
D
0
0
1

Chapter 6

2 MARKS QUESTIONS

1.Define the term fan in and fan out[2013 ,2014 ,2016]

Fan in :

It is themaximum number of inputs ,the logic gate can handle properly .

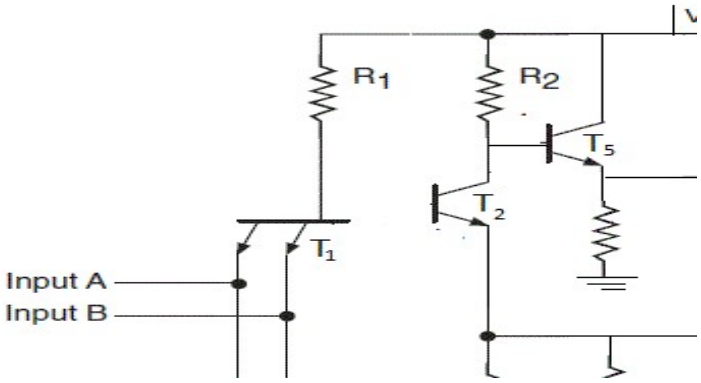
Fan out :-

The maximum number of load /similar circuits that may be simultaneously driven under worst conditions is termed as FAN out of the logic circuit .

5 MARKS QUESTIONS

1.Explain with neat sketch the working of 2 input NAND gate TTL logic family .[2014]

A TTL NAND gate is shown below :



It is clear from this figure that the transistor which normally becomes saturated are in this circuit .Schottky clamped transistors and as a result ,the storage delay or saturation delay is virtually eliminated .Which results in a better switching time .The working of this circuit is more or less such that the transistor being consumed .If e increase the values of resistance of circuit ,the switching action is fast and low power dissipation .

There will be minimum propagation delay ,when output is 1 .T4 is off (open) ,T3 is on (short) .When the output is 0 ,T4 is on ,T3 is off .The current flow from vcc to ground in this section of the circuit is minimized .If A=0 ,B=0 or both equal to 0 ,output=1 ,the base emitter diode of T1 is f.b ,saturating T1 (turning on)T2 is off ,T3 is on .If A=1 ,B=1 ,output=0 ,T1 is reverse biased ,T2 is on (turning on) .Thus T4 is on with +ve base voltage ,T3 is off.

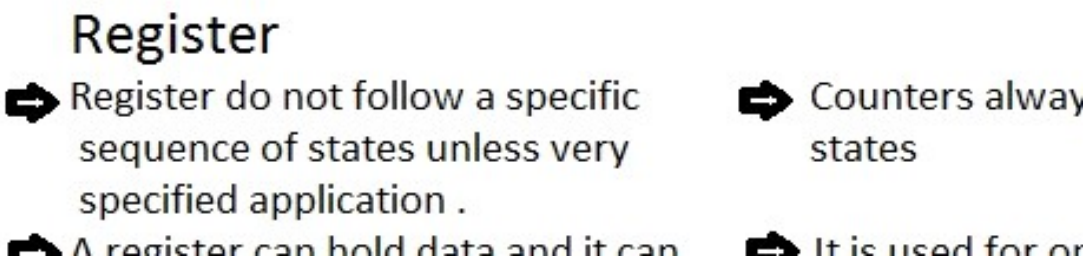
Chapter 7

2 MARKS QUESTIONS

1.Define modulous of a counter [2015,2018(w)]

Modulous of a counter is defined as equal to the number of states through which the counter progress .The maximum possible number of states is equal to 2^n ,where n=number of flipflops in the counter .

2.State 2 difference between a counter and register [2015]

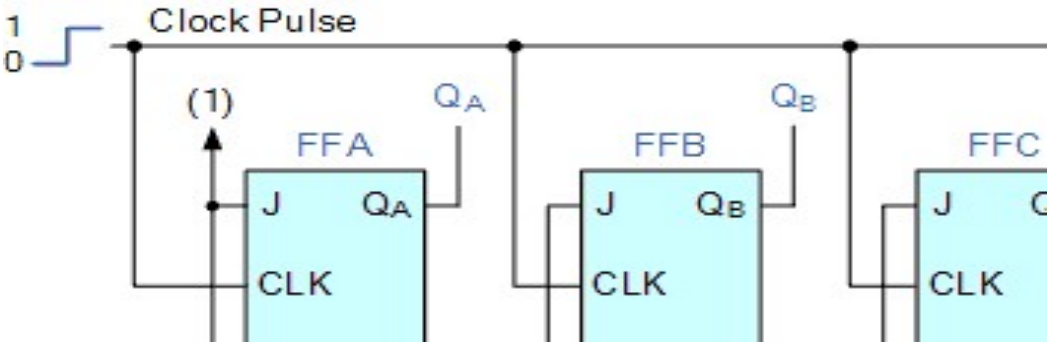


5 MARKS QUESTIONS

1.Distinguish between synchronous and asynchronous counter [2013,2018(w)]

Synchronous counter :	Asynchron
1.The clock pulse are applied to all flipflop ,hence there is minimum propagation delay	1.The delay tim .Therfore ,there delay
2.Frequency of operation can be much higher thanthat of asynchronoys counter	2.Frequency of synchronous cc
3.The maximum frequency doesnot depend on modulus	3.The maximun modulus

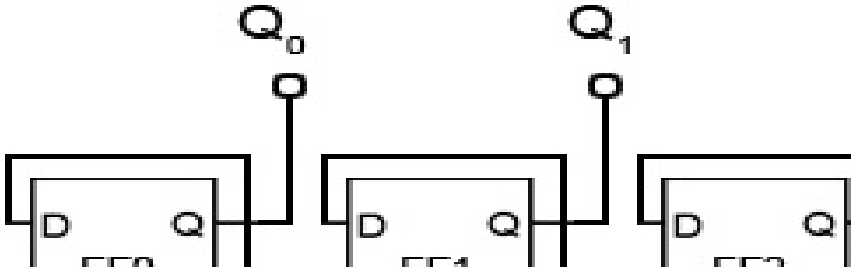
2.Design a synchronous 4 bit down counter.[2013]



As synchronous counters are formed by connecting flip-flops together and any number of flip-flops can be connected or "cascaded" together to form a "divide-by-n" binary counter, the modulo's or "MOD" number still applies as it does for asynchronous counters so a Decade counter or BCD counter with counts from 0 to 2^n-1 can be built along with truncated sequences. All we need to increase the MOD count of an up or down synchronous counter is an additional flip-flop and AND gate across it.

3.Explain briefly the working of 4 bit asynchronous up counter with neat diagram(or)/ 4-bit ripple counter.[2014,2018(w)]

Asynchronous 4-bit UP counter



A 4 bit asynchronous UP counter with D flip flop is shown in above diagram. It is capable of counting numbers from 0 to 15. The clock inputs of all flip flops are cascaded and the D input (DATA input) of each flip flop is connected to a state output of the flip flop.

That means the flip flops will toggle at each active edge or positive edge of the clock signal. The clock input is connected to first flip flop. The other flip flops in counter receive the clock signal input from Q' output of previous flip flop. The output of the first flip flop will change, when the positive edge on clock signal occurs.

In the asynchronous 4- bit up counter, the flip flops are connected in toggle mode, so when the when the clock input is connected to first flip flop FF0, then its output after one clock pulse will become 20.

The rising edge of the Q output of each flip flop triggers the clock input of its next flip flop. It triggers the next clock frequency to half of its applied input. The Q outputs of every individual flip flop (Q0, Q1, Q2, Q3) represents the count of the 4 bit UP counter

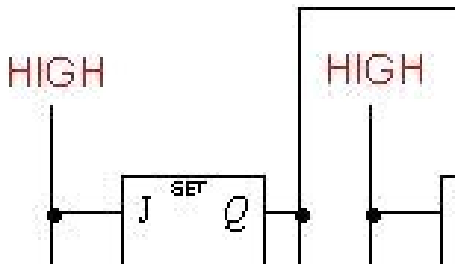
Working of asynchronous up counter is explained below,

Let us assume that the 4 Q outputs of the flip flops are initially 0000. When the rising edge of the clock pulse is applied to the FF0, then the output Q0 will change to logic 1 and the next clock pulse will change the Q0 output to logic 0. This means the output state of the clock pulse toggles (changes from 0 to1) for one cycle.

As the Q' of FF0 is connected to the clock input of FF1, then the clock input of second flip flop will become 1. This makes the output of FF1 to be high (i.e. Q1 = 1), which indicates the value 20. In this way the next clock pulse will make the Q0 to become high again.

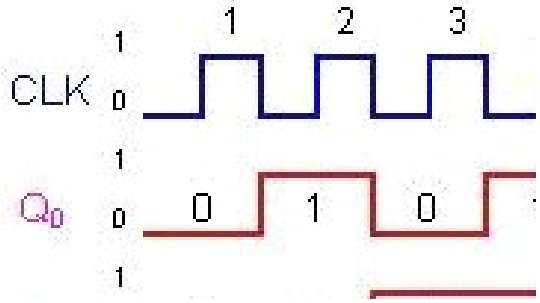
So now both Q0 and Q1 are high, this results in making the 4 bit output 11002. Now if we apply the fourth clock pulse, it will make the Q0 and Q1 to low state and toggles the FF2. So the output Q2 will become 0010¬2. As this circuit is 4 bit up counter, the output is sequence of binary values from 0, 1, 2, 3….15

4.Discuss the operation of an asynchronous counter with its timing diagram[2015]



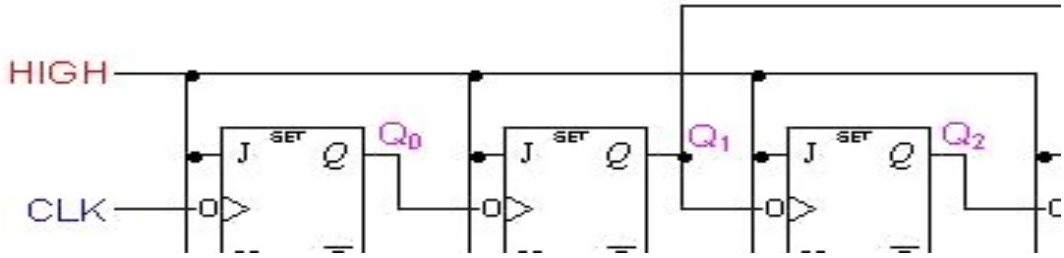
- A two-bit asynchronous counter is shown on the left. The external clock is connected to the clock input of the first flip-flop (FF0) only.
- So, FF0 changes state at the falling edge of each clock pulse, but FF1 changes only when triggered by the falling edge of the Q output of FF0.

- Because of the inherent propagation delay through a flip-flop, the transition of the input clock pulse and a transition of the Q output of FF0 can never occur at exactly the same time.
- Therefore, the flip-flops cannot be triggered simultaneously, producing an asynchronous operation.



5.Design a decade counter ,Write its truth table too [2015]

Decade counter :-



Working :-

It requires 4 T or JK flipflop .It counts from 0 to 9 again come to 0 .It has 10 states i.e 0,1,2,3,4,5,6,7,8,9 .So that it is called mod -10 counter .A binary mod-10 counter is very useful counter as it provides a means to change binary count into an equivalent count in the decimal mode .The 10 output signals can be utilised in counter tube which has grids in the form of decimal number shapes and will display the corresponding binary output in decimal number ,For decoding the 10 AND gates with 4 input for each gate .These gates work as decoding gates .For example when Q1=Q2=Q3=Q4=0 the gate will decode count 0 ,similarly count 1 can be decode by recognizing the state when Q1=Q2=Q3=Q4=1 .These 10 decoding gates will produce the designed waveform.

Chapter 8

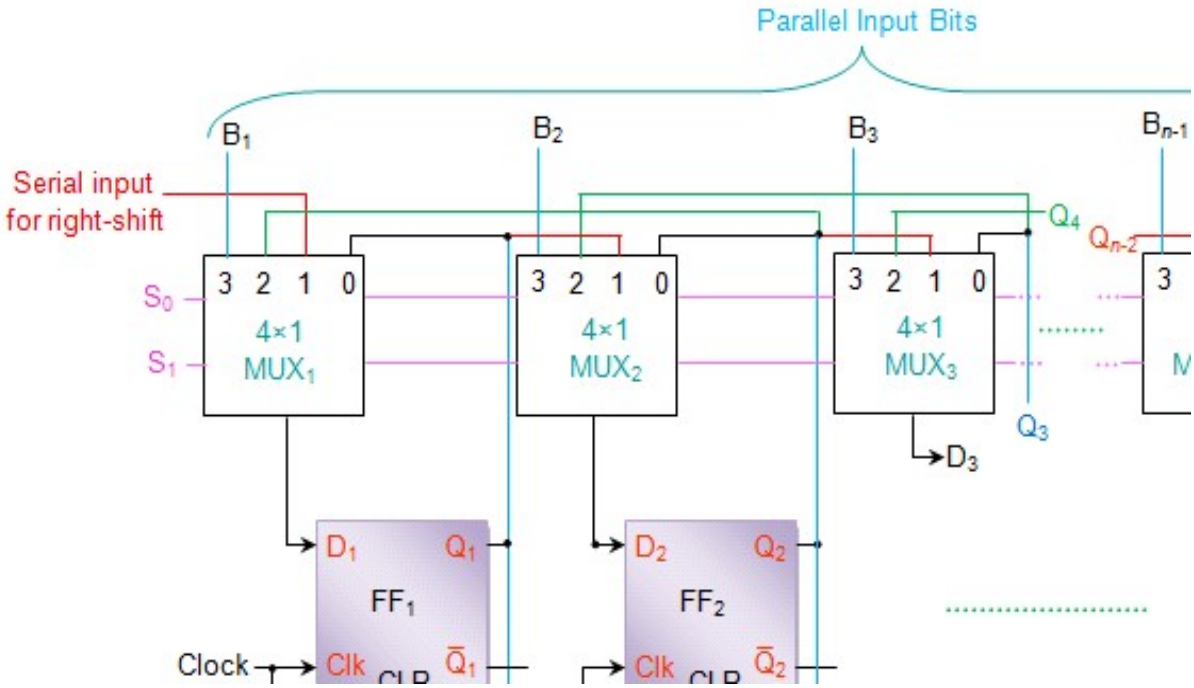
2 MARKS QUESTIONS

1.What is resister ?State its use.[2013]

Register are used to quickly accept ,store and transfer data and instructions that are being used immediately by the cpu ,there are various types of resisters,those are used for various purpose .

5 MARKS QUESTIONS

1.Explain briefly universal shift register with neat diagram .[2014]



Universal Shift Register is a register which can be configured to load and/or retrieve the data in any mode (either serial or parallel) by shifting it either towards right or towards left. In other words, a combined design of unidirectional (either right- or left-shift of data bits as in case of 4SISO, 4SIPO, 4PISO, 4PIPO) and 4bidirectional shift register along with parallel load provision is referred to as **universal shift register**. Such a 4shift register capable of storing n input bits is shown by Figure 1.

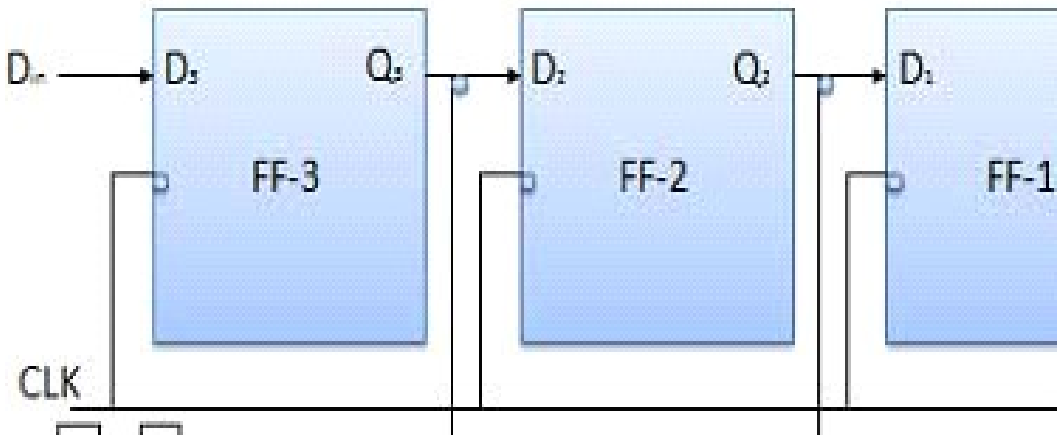
The design shown by Figure 1 uses n 4×1 multiplexers to drive the input pins of n flip-flops in the register which are also connected to clock and clear inputs. All of the 4multiplexers in the circuit share the same select lines, S_1 and S_0 (pink lines in the figure), in order to select the mode in which the shift registers operates.

2.Describe the working of a serial in parallel out shift register with the help of a suitable logic diagram[2015]

Serial in parallel out :

In this type of register the data word is entered in the register in serial way and the data is taken out parally out of the register .

In a parallel output register the output of each stage is available simultaneously .Once the data after being entered into the register ir stored in the register in its proper sequence ,each bit of the data word appears on its respective output line and all data bits are available simultaneously .



3.With a suitable logic diagram describe the working of a parallel in parallel out shift resistor[2016]

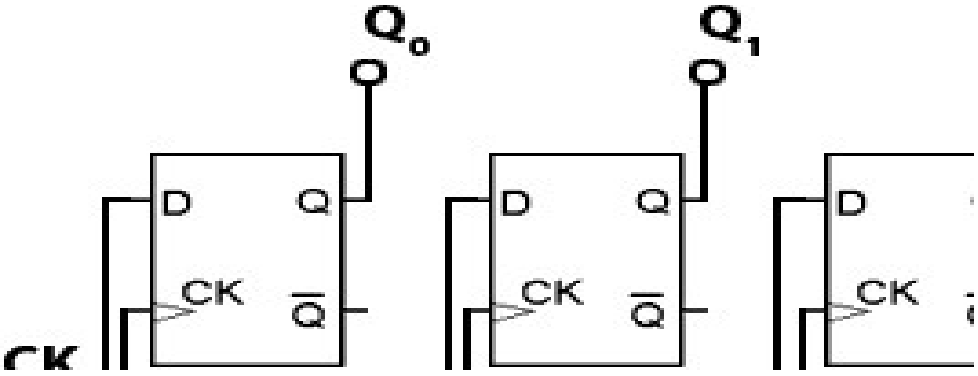
Parallel in parallel out shift register :

Parallel in parallel out shift resisters are the type of storage devices in which both data loading as well as data retrieval processes occur in parallel mode .

Fig.1 shows a pipo resister capable of storing n-bit input data word .

Here each data in appearing as its input at the instant of 1st clk pulse .

Further ,at the same instant ,the bit stored in each individual flipflop also appears at their respective output pins .



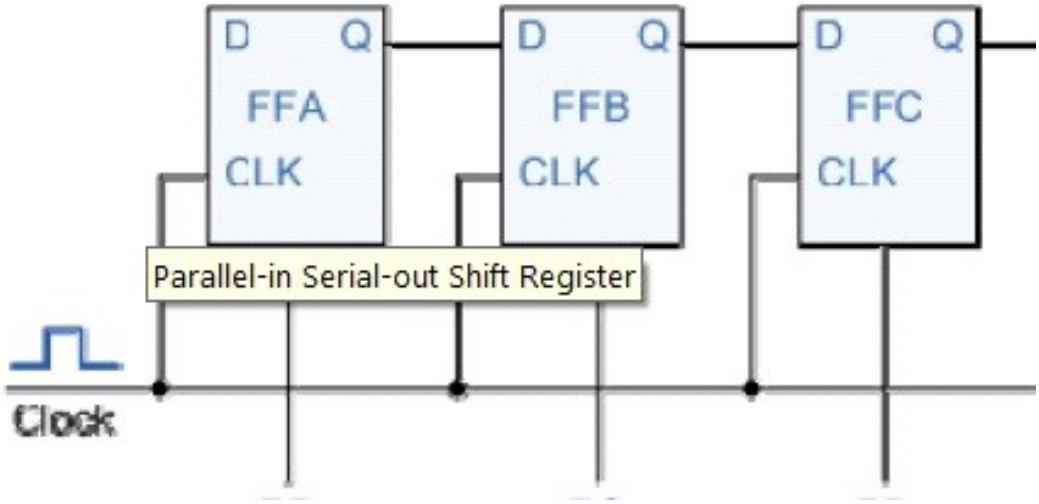
7 MARKS QUESTIONS :

1.With neat sketch explain the working of piso resistor [2013]

Parallel in serial out :

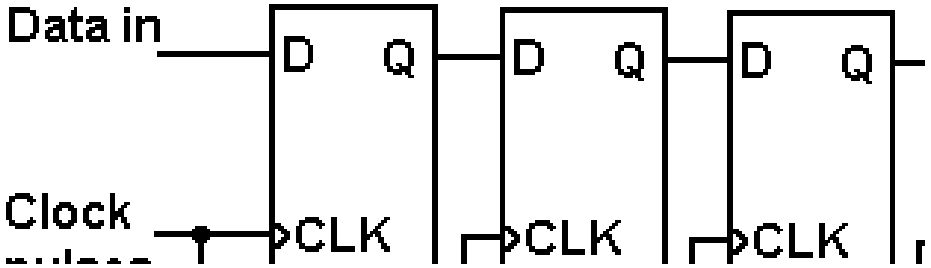
In such resistors where we have parallel input ,the data bits are entered simultaneously into their respective stages on parallel lines and not on a bit by bit basic on one lines as well the case with serial in resisters .

Serial output of these resisters are taken out the same way as siso .After the data bits are properly stored once in the resistor the data bits are taken out one by one as was the case with siso resister . Logic diagram for piso is given below .



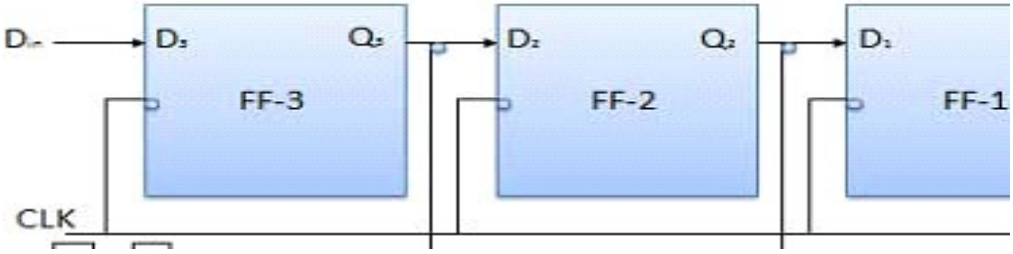
2.Explain briefly SISI ,SIPO ,PISO ,PIPO resistor .[2014,2018(w)]

SISO (Serial in serial out):-



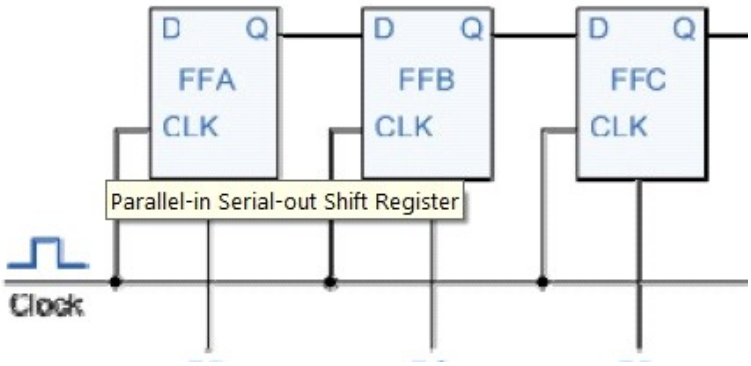
In such resistor the data is accepted serially i.e one bit at a time is accepted on a line .The stored information is also produced at the output in serial form

SIPO(Serial in parallel out):-



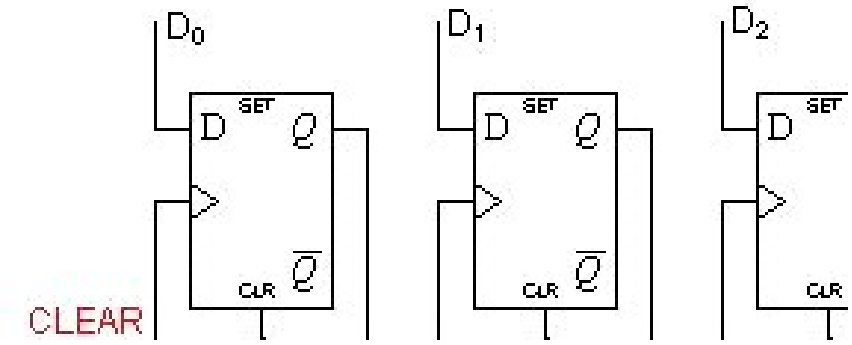
In this type of resistor the data entered in the resistor in serial way and the data is taken out of the resistor in parallel way simultaneously .

PISO (Parallel inpserial out):-



In this type of resister the data are entered in parallel way simultaneously and out in serial way .

PIPO (Parallel in parallel out):-



Here data is given in parallel way simultaneously to all flipflops and also data is out in parallel way simultaneously .

Chapter 9

1.Define resolution of 8 bit of DAC .[2013]

- The resolution of digital to analog converter is the measure of how finely its output may change between discrete ,binary steps .
- For instance ,an 8-bit DAC with an output voltage range of 0 to 10 volts will have a resolution of 39.22mv

2.Write the difference between weighted resister DAC and R-2R DAC converter [2014]

Comparison of Weighted R & R-2R Ladc

Weighted Resistor DAC	R-2R La
1. Simple Construction	1. Slightly
2. Wide range of resistors are required	2. Resistc require
3. One resistors per bit are required	3. Two r require

5 MARKS QUESTIONS

1.Explain the operation of 7 segment display .[2013,2018(w)]

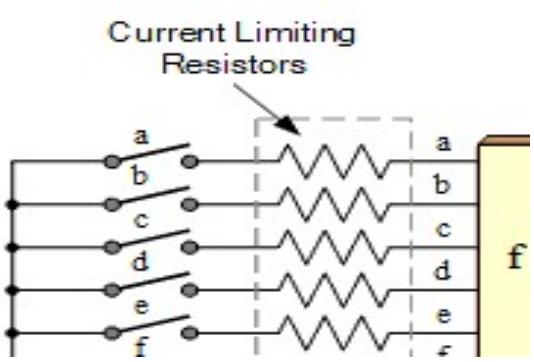
- An LED or Light Emitting Diode, is a solid state optical PN-junction diode which emits light energy in the form of "photons" when it is forward biased by a voltage allowing current to flow across its junction, and in Electronics we call this process electroluminescence.
- The actual colour of the visible light emitted by an LED, ranging from blue to red to orange, is decided by the spectral wavelength of the emitted light which itself is dependent upon the mixture of the various impurities added to the semiconductor materials used to produce it.
- Light emitting diodes have many advantages over traditional bulbs and lamps, with the main ones being their small size, long life, various colours, cheapness and are readily available, as well as being easy to interface with various other electronic components and digital circuits.
- But the main advantage of light emitting diodes is that because of their small die size, several of them can be connected together within one small and compact package producing what is generally called a **7-segment**

Display.

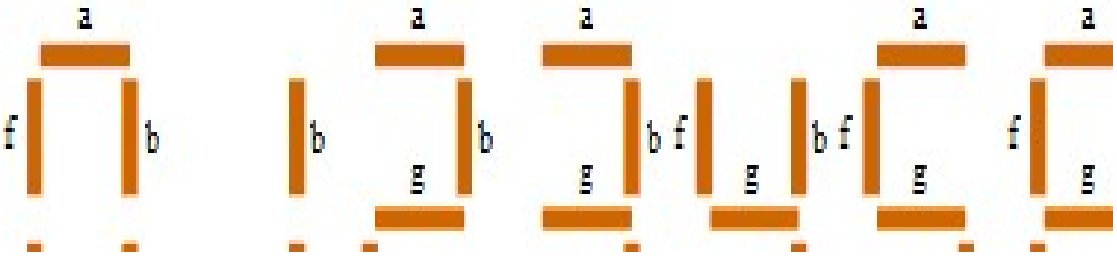
- The *7-segment display*, also written as "seven segment display", consists of seven LEDs (hence its name) arranged in a rectangular fashion as shown.

- Each of the seven LEDs is called a segment because when illuminated the segment forms part of a numerical digit (both Decimal and Hex) to be displayed. An additional 8th LED is sometimes used within the same package thus allowing the indication of a decimal point, (DP) when two or more 7-segment displays are connected together to display numbers greater than ten.

Driving a 7-segment Display



7-Segment Display Segments for all Numbers.



. Then for a 7-segment display, we can produce a truth table giving the individual segments that need to be illuminated in order to produce the required decimal digit from 0 through 9 as shown below.

7-segment Display Truth Table

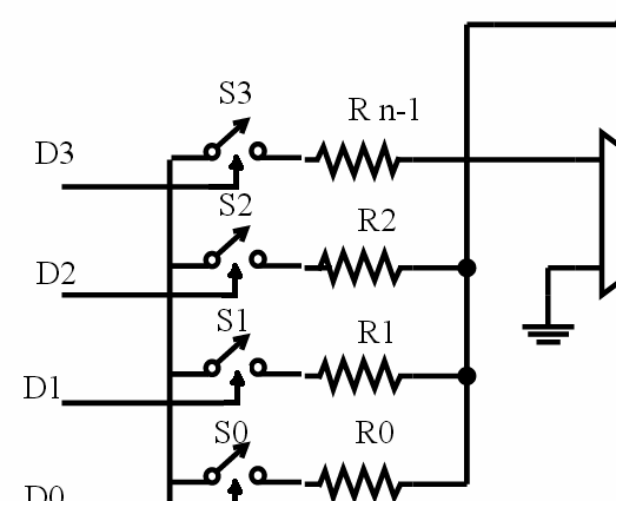
Decimal Digit	Individual Segments Illuminated						
	a	b	c	d	e	f	g
0	×	×	×	×	×	×	
1		×	×				
2	×	×		×	×		×
3	×	×	×	×			×
4		×	×			×	×
5	×		×	×		×	×
6	×		×	×	×	×	×
7	×	×	×				
8	×	×	×	×	×	×	×
9	×	×	×			×	×

2.Explain the binary weighted type of D/A converter with neat sketch [2013 ,2014 ,2016]

Weighted Resistor DAC and its Operation

Many times we require to convert a digital output into its equivalent analog voltage. To perform this operation we are going to use weighted resistor digital to analog converter.

The following figure shows the circuit diagram of weighted resistor DAC. This DAC circuit uses weighted values of resistor like 2R, 4R, 6R, 8R and so on depending on the digital inputs available therefore such type of network is known as weighted resistor DAC.



This circuit consists of a transistor switch (shown by the upward arrow) which turns on the switch when the digital input is '1' and if digital input becomes '0' it will open the switch. When transistor switch gets closed, current flows through the weighted resistor due to the reference voltage as shown in circuit diagram.

When all such currents from different weighted resistors get added at summing point (which is also known as a virtual ground) of the operational amplifier it will produce a proportional voltage as its output.

For a 4 bit DAC, the output V0 is given as follows

$$V_o = -V_{ref}\left(S_3 \times \frac{Rf}{R3} + S_2 \times \frac{Rf}{R2} + S\right.$$

Where S3, S2, S1 and S0 represents the status of the switches i.e. on or off (1 or 0).

f resistors are in binary weights i.e. R3=2Rf, R2=4Rf, R1=8Rf and R0=16Rf, the above equation can be written as,

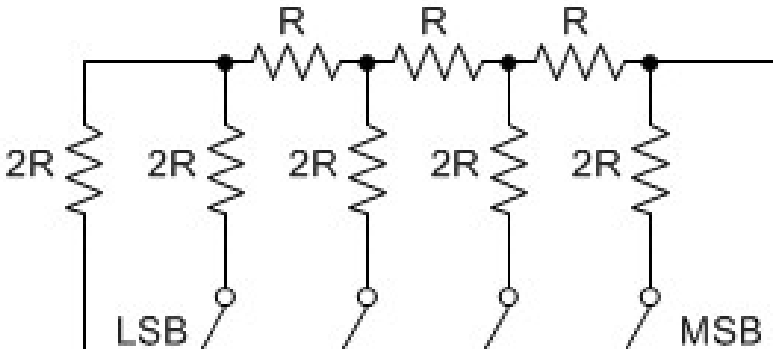
$$V_o = -V_{ref}\left(\frac{S3}{2^1} + \frac{S2}{2^2} + \frac{S1}{2^3} + \frac{S0}{2^4}\right)$$

From the above discussion, we can say that for a 4 bit DAC 4 switches produces 16 different combinations of output and hence produces 16 different output voltage.in general n-bit DAC produces 2^n different discrete analog voltages.

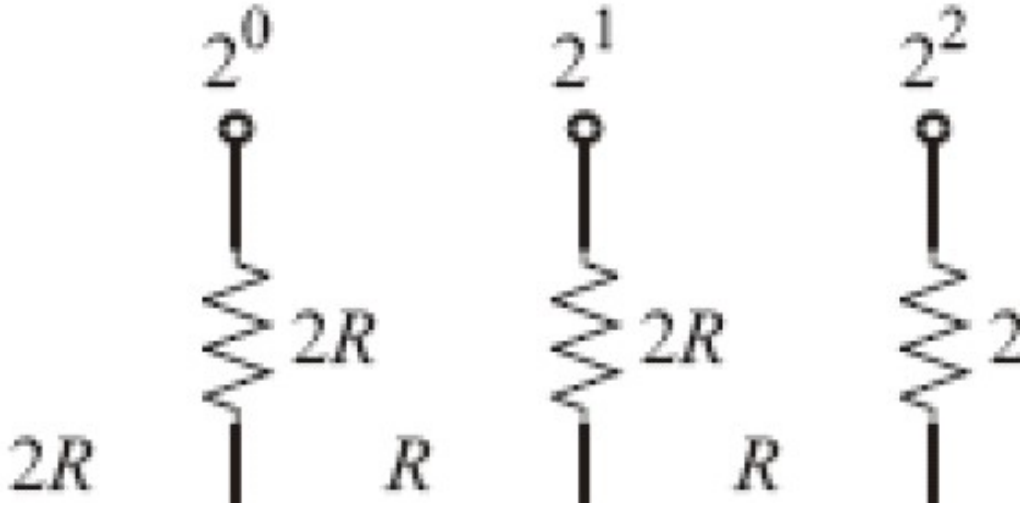
3.Explain the working of a R-2R ladder network type D/A converter with diagram [2015]

Ladder type D/A converter :

Let us consider a ladder network R/2R network for D/A as shown in the given figure .



When switch S1 is switched ON to ref. Voltage and S2 ,S3 and S4 are ground .The network becomes as shown in fig. Given below .



Now looking down from pt. A the resistance is 2R , looking up from pt.A it is 2R .Hence the total resistance seen by pt.A is 3R .Looking down and left and D we have two resistances in parallel of 2R which means we have a resistance of R only ,When looking down from D .Now we have resistance R between C and D so looking at C we have resistance of 2 R .In this wy at pt. B ,A the resistances are calculated as a ladder

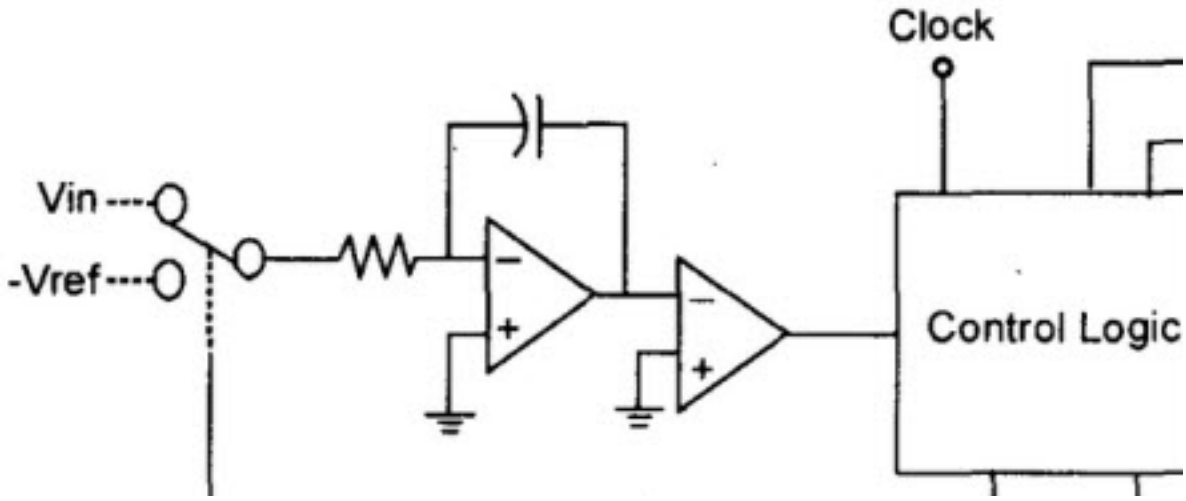
Total resistance seen by point is 3R

Total current=

7 MARKS QUESTIONS

1.Explain the working of dual slope type A/D converter with neat sketch[2013 ,2014]

These type of converters do not use D/A converter instead of this they use linear ramp generator to produce constant reference voltage .



Now consider that the output of the integrator is zero and the counter is reset .Now if we assume that +ve input voltage is applied to the input through the switch s and constant for a period of time .There will be a constant current flow through the resistance .As the current is constant ,the capacitor will be charged linearly as a result of this charging there will be a –ve linear voltage from the output integrator .

After a certain interval of time or when count reaches a specified counter will reset and the –ve reference voltage $-V_{ref}$ will be switched at the integrator .

Now,the capacitor is charged to a –ve voltage proportional to the input analog voltage .

Due to the constant current from the $-V_{ref}$ the capacitor discharges linearly .This discharge produces a +ve ramp of the integrator .

As the capacitor discharges the counter which was initially reset ,starts counting finally when the integrator switches off the clock and send a signal to the counter .After completion of one cycle the binary count is latched .